CLAIMS

What is claimed is:

1. A multi-channel analog front end comprises:

system clock module operable to produce a system clock;

first channel path operable to process first data in a domain conversion, wherein the first channel path includes:

first sample rate converter operably coupled to convert a frequency of the first data from a first channel frequency to a second frequency based on a first integer ratio of the system clock and the first channel frequency; and

first domain conversion module converts domain of the first data from a first domain to a second domain;

second channel path operable to process second data in the domain conversion, wherein the second channel path includes:

second sample rate converter operably coupled to convert a frequency of the second data from a second channel frequency to the second frequency based on a second integer ratio of the system clock and the second channel frequency; and

second domain conversion module converts domain of the second data from the first domain to the second domain.

2. The multi-channel analog front end of claim 1 further comprises:

third channel path operable to process third data in an inverse domain conversion, wherein the third channel path includes:

third sample rate converter operably coupled to convert a frequency of the third data from the second frequency to a third channel frequency based on a third integer ratio of the system clock and the third channel frequency; and

third domain conversion module converts domain of the third data from the second domain to the first domain;

fourth channel path operable to process fourth data in the inverse domain conversion, wherein the fourth channel path includes:

fourth sample rate converter operably coupled to convert a frequency of the fourth data from the second frequency to a fourth channel frequency based on a fourth integer ratio of the system clock and the fourth channel frequency; and

fourth domain conversion module converts domain of the fourth data from the second domain to the first domain.

3. The multi-channel analog front end of claim 1 further comprises:

a control module operably coupled to determine the first and second integer ratios of the system clock based on the second frequency and the frequencies of the first and second data, respectively.

4. The multi-channel analog front end of claim 3, wherein the first sample rate converter further comprises:

receiver module operably coupled to receive a word of the first data and to store the word to produce a stored word; and

rate conversion module operably coupled to retrieve the stored word and to replicate the stored word based on the first integer ratio of the system clock to produce a sample rate converted word.

5. The multi-channel analog front end of claim 4, wherein the rate conversion module further comprises:

integer rate conversion module operably coupled to produce integer replications of the stored word to produce the sample rate converted word.

6. The multi-channel analog front end of claim 4, wherein the rate conversion module further comprises:

interpolative rate conversion module operably coupled to produce at least one replication of the stored word and an interpolated representation of the stored word to produce the sample rate converted word.

7. The multi-channel analog front end of claim 3, wherein the second sample rate converter further comprises:

receiver module operably coupled to receive a word of the second data and to store the word to produce a stored word; and

rate conversion module operably coupled to retrieve the stored word and to replicate the stored word based on the second integer ratio of the system clock to produce a sample rate converted word.

8. The multi-channel analog front end of claim 7, wherein the rate conversion module further comprises:

integer rate conversion module operably coupled to produce integer replications of the stored word to produce the sample rate converted word.

9. The multi-channel analog front end of claim 7, wherein the rate conversion module further comprises:

interpolative rate conversion module operably coupled to produce at least one replication of the stored word and an

interpolated representation of the stored word to produce the sample rate converted word.

10. The multi-channel analog front end of claim 1, wherein the each of the first and second domain conversion modules further comprises at least one of: an analog to digital converter and a digital to analog converter.

11. The multi-channel analog front end of claim 1, wherein the each of the first and second domain conversion modules further comprises a filtering module operably coupled to filter the first and second data respectively.

12. A method for providing domain conversion for multiple channels, the method comprises the steps of:

generating a system clock;

converting a frequency of first data from a first channel frequency to a second frequency based on a first integer ratio of the system clock and the first channel frequency;

converting domain of the first data from a first domain to a second domain;

converting a frequency of second data from a second channel frequency to the second frequency based on a second integer ratio of the system clock and the second channel frequency; and

converting domain of the second data from the first domain to the second domain.

13. The method of claim 12 further comprises:

converting a frequency of the third data from a third channel frequency to the second frequency based on a third integer ratio of the system clock and the third channel frequency;

converting domain of the third data from the second domain to the first domain;

converting a frequency of the fourth data from a fourth channel frequency to the second frequency based on a fourth

integer ratio of the system clock and the fourth channel frequency; and

converting domain of the fourth data from the second domain to the first domain.

14. The method of claim 12 further comprises:

determining the first and second integer ratios of the system clock based on the second frequency and the frequencies of the first and second data, respectively.

15. The method of claim 14, wherein the converting the domain of the first and second data from the first domain to the second domain further comprises:

storing a word of the first and second data to produce a stored word; and

replicating the stored word based on the first and second integer ratios to produce a sample rate converted word, respectively, based on at least one of: an integer replication and an interpolation replication.

16. An apparatus for providing domain conversion for multiple channels, the apparatus comprises:

processing module; and

memory operably coupled to the processing module, wherein the memory includes operational instructions that cause the processing module to:

generate a system clock;

convert a frequency of first data from a first channel frequency to a second frequency based on a first integer ratio of the system clock and the first channel frequency;

convert domain of the first data from a first domain to a second domain;

convert a frequency of second data from a second channel frequency to the second frequency based on a second integer ratio of the system clock and the second channel frequency; and

convert domain of the second data from the first domain to the second domain.

17. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to:

convert a frequency of the third data from a third channel frequency to the second frequency based on a third integer ratio of the system clock and the third channel frequency;

convert domain of the third data from the second domain to the first domain;

convert a frequency of the fourth data from a fourth channel frequency to the second frequency based on a fourth integer ratio of the system clock and the fourth channel frequency; and

convert domain of the fourth data from the second domain to the first domain.

18. The apparatus of claim 16, wherein the memory further comprises operational instructions that cause the processing module to:

determine the first and second integer ratios of the system clock based on the second frequency and the frequencies of the first and second data, respectively.

19. The apparatus of claim 18, wherein the memory further comprises operational instructions that cause the processing module to convert the frequency of the first and second data from the first and second channel frequencies to the second frequency, respectively, by:

storing a word of the first and second data to produce a stored word; and

replicating the stored word based on the first and second integer ratios to produce a sample rate converted word, respectively, based on at least one of: an integer replication and an interpolation replication.